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Sixth Semester B.E. Degree Examination, June/July 2019
Microelectronics

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a. Derive the expression of drain current of a MOS device for triode and saturation region.
       (08 Marks)

   b. Consider a CMOS process for which $L_{min} = 0.4\mu m$, $t_{ox} = 8nm$, $\mu_n = 450cm^2/v.s$ and $v_t = 0.7V$

   i)   Find C_{ox} and $k_n^!$

   ii) For an NMOS transistor $\dfrac{W}{L} = \dfrac{8\mu m}{0.8\mu m}$. Calculate the values of V_{GS} and V_{DSmin} needed to operate a transistor in saturation region with a DC current $I_D = 100\mu A$.

   iii) For the derive in (ii), find the value of V_{GS} required to cause the device to operate as 1000Ω resistor for a very small V_{DS}.
        (08 Marks)

OR

2   a. With the neat diagram obtain the expression for finite O/P resistance in saturation region.
       (07 Marks)

   b. Define the following parameter with respect to MOSFET:
      i) Threshold voltage   ii) Body Effect.
      (05 Marks)

   c. For the circuit shown in Fig.Q.2(c), find the values of R and V_D to obtain a current I_D of $80\mu A$. Let the NMOS transistor have $V_t = 0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $L = 0.8\mu m$ and $W = 4\mu m$. Assume $\lambda = 0$.
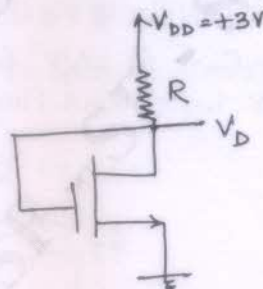   **(04 Marks)**

Fig.Q.2(c)

Module-2

3   a. Draw the circuit diagram of source follower amplifier. Draw its small signal equivalent circuit with r_o. Obtain the expression for R_{in}, R_{out}, A_v, A_{v_o} and Gv.
       (10 Marks)

   b. List the various techniques used for biasing in MOS amplifier circuits and explain any two in detail.
      (06 Marks)

OR

8 a. Explain the following: i) Double cascode   ii) Folded cascode. **(08 Marks)**
   b. Explain the high frequency response of MOS cascode amplifier with necessary diagram and expressions. **(08 Marks)**

Module-5

9 a. Explain the operation of MOS differential pair with a differential input voltage. **(08 Marks)**
   b. Prove that $A_{CM} = \dfrac{-r_{04}}{2R_{ss}} \times \dfrac{1}{1+g_{m3}r_{o3}}$ for the active loaded MOS differential amplifier.

   (08 Marks)

OR

10 a. For the nMOS differential pair with a common mode voltage V_{CM} applied as shown in Fig.Q.10(a). Let $V_{DD} = V_{SS} = 2.5V$ $K_n^! \dfrac{W}{L} = 3mA/v^2$, $V_{tn} = 0.7V$, $I = 0.2mA$, $R_D = 5K\Omega$.

   Neglect channel length modulation
   i)   Find V_{OV} and V_{GS} for each transistor
   ii)   For $V_{CM} = 0$, Find Vs, i_{D1}, i_{D2}, V_{D1} and V_{D2}
   iii) What is highest value of V_{cm} for which Q_1 and Q_2 remain in saturation, if current source I requires a minimum voltage of 0.3V to operate properly. What is the lowest value for V_s and hence for V_{cm}?
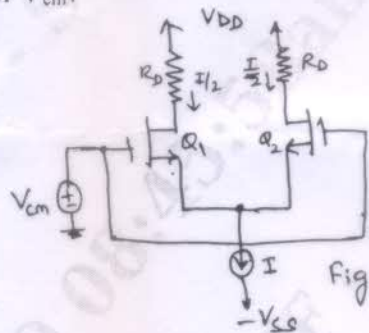

Fig.Q.10(a)

(08 Marks)

   b. With neat circuit diagram, explain the operation of two stage CMOS Op-amp configuration. **(08 Marks)**

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